REMARKS

In the Office Action mailed September 1, 2005 claims 1-27 were rejected. Reconsideration and allowance of all pending claims are requested.

Rejections Under 35 U.S.C. § 102

The Examiner rejected claims 1, 4, 5, 7, 10-13, 15-17 and 20 under 35 U.S.C. § 102(e) as being anticipated by Lucas et al. (U.S. Patent No. 6,294,820, hereinafter "Lucas"). Applicants submit that all of the claims are distinguishable over Lucas. In particular, independent claims 1 and 17 specifically recite filling a trench by conformally depositing an optically isolating material, which is neither taught nor suggested by Lucas.

Lucas fails to teach a trench in which an optical isolating material is disposed.

Lucas teaches a semiconductor device comprising trench isolation regions. These trench regions are lined with an electrically insulating layer 14 (Fig. 1), for example a silicon dioxide layer. Lucas also teaches the use of the silicon dioxide layer 14 over which tetraethylorthosilicate (TEOS) is deposited (dielectric trench fill 16). There is no mention made that the TEOS is an optically isolating material. Indeed, the reference does not even mention optical isolation. Moreover, neither the reference nor the Examiner has provided any objective evidence that TEOS on silicon dioxide would or could serve as an optical isolating material.

The Examiner would read col. 3, lines 44 - 49 as indicating that the polysilicon could be substituted for the TEOS. However, the reference does *not* teach that substitution, but merely the substitution of *the entire structure of Fig. 1* with polysilicon buffer local oxidation of silicon (LOCOS).

It is well known that the polysilicon in polysilicon buffer LOCOS is used for stress relief and *not* for optical isolation. The resulting structures are not similar to those

of claim 1 or claim 17. For example, in U.S. Patent No. 5,192,707, col. 1, lines 47-56 provides:

> To reduce the bird's beak effect, there has been proposed the use of a polysilicon layer between the nitride layer and the pad oxide layer as more fully described in U.S. Pat. No. 4,407,696 issued Oct. 4, 1983 to Han et al. The use of the polysilicon layer in the LOCOS process, known as poly-buffered LOCOS, is used to reduce oxidation induced stacking faults resulting from the stress caused by the different thermal coefficients of expansion between the silicon substrate and a thick silicon nitride layer overlying the substrate.

Processes such as LOCOS and polysilicon buffer LOCOS do not provide optical isolation. Therefore, Lucas teaches a material and structure that has not been demonstrated by either Lucas or the examiner as capable of providing the claimed optical isolation.

The shallow trench isolation (STI) process taught by Lucas is precisely the non-optically isolating technique improved upon by the invention.

Lucas specifically characterizes the arrangement of Fig. 1 as "shallow trench isolation" or "STI" (see col. 3, lines 44-45). It is known that STI does NOT provide optical isolation. Indeed, it is this problem with STI that the claimed invention addresses. As mentioned on page 1, paragraph 2 of the application:

> A number of solutions to electrically isolate adjacent devices are available, including local oxidation of silicon (LOCOS), shallow trench isolation (STI) and deep trench isolation (DTI). When properly designed, these isolation structures can reduce unwanted diffusion of dopants, prevent and/or reduce capacitance coupling, or prevent latch-up between adjacent devices. However, these solutions do not provide any optical isolation between adjacent devices.

Therefore, the process shown in Fig. 1 and described by Lucas actually represents the prior art STI that the invention is intended to improve upon, by providing optical isolation.

Applicants therefore submit that Lucas cannot anticipate claim 1 or claim 17, or the claims depending therefrom.

Rejections Under 35 U.S.C. § 103

The Examiner rejected claims 6 and 22 under 35 U.S.C. §103(a) as being unpatentable over Lucas in view of Seitz (U.S. Patent Application No. 2003/0013270). The Examiner also rejected claims 8, 9, 21, 23 and 24-27 under 35 U.S.C. §103(a) as being unpatentable over Lucas in view of Wensley et al. (U.S. Patent Application No. 2004/0175897). The Examiner further rejected claim 14 under 35 U.S.C. §103(a) as being unpatentable over Lucas in view of Takaishi et al. (U.S. Patent Application No. 6,239,001).

All of these claims depend directly or indirectly on allowable base claims 1 or 17. Accordingly, these claims are believed to be clearly patentable at least by virtue of their dependency from the allowable base claims.

Conclusion

In view of the remarks and amendments set forth above, Applicants respectfully request allowance of the pending claims. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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